FB4-DMX WPISO

Isolated DMX512 receiver module · 46 × 24 mm

Datasheet Rev A
Board revision 260820
Marking: FB4 DMX WPISO / 20.Aug.2026
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1 Description

The FB4-DMX WPISO is a compact, galvanically isolated DMX512 receive front end for LED fixtures, lighting controllers and effect equipment. It runs from a single 3.3 V rail supplied by the host and hands the received DMX bit stream to the host as a plain 3.3 V CMOS UART signal, while the entire DMX side — transceiver, protection network and cable common — floats with respect to host ground.

The isolated side is powered by an on-board converter, so no second supply rail and no external isolated DC/DC module are required on the host board.

An I²C control interface is provided on the same connector. One port bit is hard-wired low inside the module, giving the host a positive module-present / identification read over the two-wire bus it already uses.

The module receives only: the transceiver's driver is permanently disabled and its receiver permanently enabled, so the module can never talk back onto the DMX line.

2 Features

- Galvanically isolated DMX512-A / RS-485 receive path
- On-board isolated 3.3 V supply — single 3.3 V input, no external isolated rail
- Receive-only by hardware; the driver cannot be enabled
- ±15 kV ESD-rated transceiver, 1/8 unit load (256 nodes per bus)
- On-board TVS and series protection on the DMX pair, qualified to IEC 61000-4-2/-4/-5
- Fail-safe biasing: bus open, shorted or unterminated → defined idle (MARK) output
- Cable common (SGND) resistively referenced to isolated ground
- I²C control interface with open-drain interrupt
- Two status LEDs: host 3.3 V present, isolated 3.3 V present
- 46 × 24 mm, 2 × M3 mounting holes on 38 mm centres
- –25 °C to +85 °C operating

Applications

- Architectural and stage LED fixtures
- Moving heads, effect and haze machines
- DMX-controlled drivers, dimmers and relay packs
- Retrofit of a DMX input onto an existing 3.3 V controller

Key specifications at a glance

Supply	3.0–3.6 V single rail from the host; the isolated rail is generated on board
Host interface	UART data out (RO) + I²C control · 7-pin ZH 1.5 mm connector
DMX interface	DMX512-A / RS-485 receive, 250 kbit/s, 1/8 unit load, on-board transient protection · 3-pin XH 2.5 mm connector
Isolation	Functional; barrier type-tested to 3.75 kV_{rms} / 3 kV_{rms} (1 min) — see §6
Mechanical	46.0 × 24.0 mm, 2 × M3 · –25 °C to +85 °C

> **Notice — preliminary data**
>
> This document describes board revision 260820 as built. Values marked † are calculated and have not yet been confirmed by bench measurement. The module is a sub-assembly intended for integration into end products; the integrator is responsible for the compliance of the finished equipment. Specifications are subject to change without notice.

3 Connectors and pin functions

3.1 J2 — host interface

JST ZH series, 1.5 mm pitch, 7 positions, vertical SMD with two solder tabs. Mates with a ZHR-7 housing and SZH-002T-P0.5 crimp contacts (or equivalent). Rated 1 A / 100 V per contact.

Pin	Legend	Name	Type	Function
1	V	+3.3V	Power	Module supply input, 3.0–3.6 V
2	INT	INT	Open-drain out	Interrupt, active low. External pull-up required.
3	SDA	SDA	Open-drain I/O	I²C data. External pull-up required.
4	SCL	SCL	Input	I²C clock. External pull-up required.
5	DI	—	—	**Not connected on this revision.** The legend is reserved for a future transmit-capable build; leave open.
6	RO	RO	Output	Received DMX bit stream, 3.3 V CMOS, idle high (MARK)
7	G	GND	Power	Host ground
tabs	—	GND	Mechanical	Two solder tabs, tied to GND

3.2 J1 — DMX input

JST XH series, 2.5 mm pitch, 3 positions, vertical SMD with two board posts. Mates with an XH-3Y housing and SXH-001T-P0.6 crimp contacts (or equivalent). Rated 3 A / 250 V per contact. Silkscreen legend “3 / 2 / 1”.

Pin	Name	DMX512 XLR-5	Function
1	Data+	pin 3	Non-inverting bus line. Transient-protected and fail-safe biased on board.
2	Data–	pin 2	Inverting bus line. Transient-protected and fail-safe biased on board.
3	SGND	pin 1	Cable common / shield reference. Resistively coupled to the module's isolated ground — not a direct connection.
posts	GND-ISO	—	Two mechanical posts, tied to isolated ground

3.3 Status indicators

Reference	Colour	Meaning
LED1	Green	Host 3.3 V rail present (lit whenever J2-1 is powered)
LED2	Green	Isolated 3.3 V rail present, i.e. the internal converter is running

Both indicators run at very low current by design. They are a production and service aid rather than a user-facing indicator: they are dim, and dimmer still at low temperature.

4 Absolute maximum ratings

Stresses beyond these values may cause permanent damage. These are stress ratings only; functional operation at these limits is not implied.

Parameter	Min	Max	Unit
Supply voltage, J2-1 (+3.3V) to GND	−0.3	4.0	V
Voltage on SDA, SCL, INT, RO to GND	−0.3	V_{CC} + 0.3	V
Continuous voltage, J1-1 / J1-2 to J1-3 (SGND)	−12	+12	V
ESD on DMX pins, human body model	−15	+15	kV
Continuous voltage across the isolation barrier — see §6	−42	+42	V_{DC}
Storage temperature	−40	+85	°C

5 Recommended operating conditions and electrical characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage V_{CC}	J2-1	3.0	3.3	3.6	V
Supply current I_{CC} †	DMX line active, LEDs on	—	5	20[1]	mA
Operating ambient temperature[2]	—	−25	—	+85	°C
I²C clock frequency	—	—	100	400	kHz
DMX data rate	DMX512-A	—	250	500	kbit/s
DMX receiver input impedance	1/8 unit load, 256 nodes per bus	96	—	—	kΩ
RO output high level	I_{OH} = −2 mA	V_{CC} − 0.4	—	—	V
RO output low level	I_{OL} = 2 mA	—	—	0.4	V
RO recommended load current	continuous, either direction	—	—	±2	mA
Barrier propagation delay	bus receiver output → J2-6	—	8	—	ns
Common-mode transient immunity	across the barrier	100	—	—	kV/µs

1. Recommended supply budget for the host, not a measured maximum.
2. Limited by the wire-to-board connectors. All active devices are rated −40 °C or wider.

† Calculated; bench verification pending. V_{CC} = 3.3 V, T_A = 25 °C unless stated otherwise.

6 Isolation

Parameter	Value
Isolation type	Functional / galvanic separation of the DMX port from host ground
Signal path, UL 1577 type test	3750 V_{rms}, 1 minute
Signal path, continuous working voltage	400 V_{rms} / 566 V_{pk}, basic grade
Power path, type test	3000 V_{rms}, 1 minute
Minimum PCB clearance / creepage across the barrier	0.26 mm top layer, 0.76 mm bottom layer
Recommended maximum continuous barrier voltage	30 V_{rms} / 42 V_{DC}

> **Read this before you rely on the barrier**
>
> The isolation components are rated for kilovolt type tests, but on this module the *limiting element is the printed circuit board*: the narrowest gap across the barrier is 0.26 mm on the top layer. The module therefore provides **functional isolation only** — it breaks ground loops between the DMX line and the host, and it survives the common-mode transients that DMX cabling produces. It is **not** rated for basic or reinforced isolation from mains, and it must not be used as a safety barrier. Both domains must be SELV / ES1 circuits. Keep the barrier region clean, dry and free of conductive debris; do not run host-board copper or wiring across it.

7 Functional description

7.1 DMX front end

The pair arrives at J1 and passes a bidirectional TVS network referenced to the cable common on J1-3, qualified to IEC 61000-4-2, -4-4 and -4-5. Each line then reaches the RS-485 receiver inputs through series protection, so the protection network takes the surge energy before it can reach the silicon. On-board bias holds the pair in the idle state when no transmitter is driving the line; together with the transceiver's own fail-safe circuit this guarantees RO = high for an open, shorted or idle bus.

The receiver is slew-rate limited and presents 1/8 unit load, so up to 256 modules may share one DMX line as far as the electrical layer is concerned.

7.2 Isolated data path

The receiver output crosses the barrier through a capacitive digital isolator with an 8 ns typical propagation delay, 100 kV/µs common-mode transient immunity and a default-high fail-safe output. At the 250 kbit/s DMX rate the barrier contributes no meaningful delay or jitter.

7.3 Isolated power

An on-board push-pull converter and isolation transformer generate the isolated rail, which is rectified and used only inside the module. The rail is unregulated and is dimensioned for the receiver, the bias network and the indicator; it is not brought out to either connector.

7.4 Host interface and control

RO is a plain 3.3 V CMOS output; connect it to a UART receive pin configured for 250 kbit/s, 8 data bits, no parity, 2 stop bits. Detect the DMX BREAK either as a framing error or with a timer on the low period.

The control interface is I²C at up to 400 kHz with an open-drain interrupt line. One port bit is hard-wired low inside the module and reads back as a module-present / identification check. The device address, register map and the recommended initialisation sequence are supplied with the integration notes.

8 Typical application

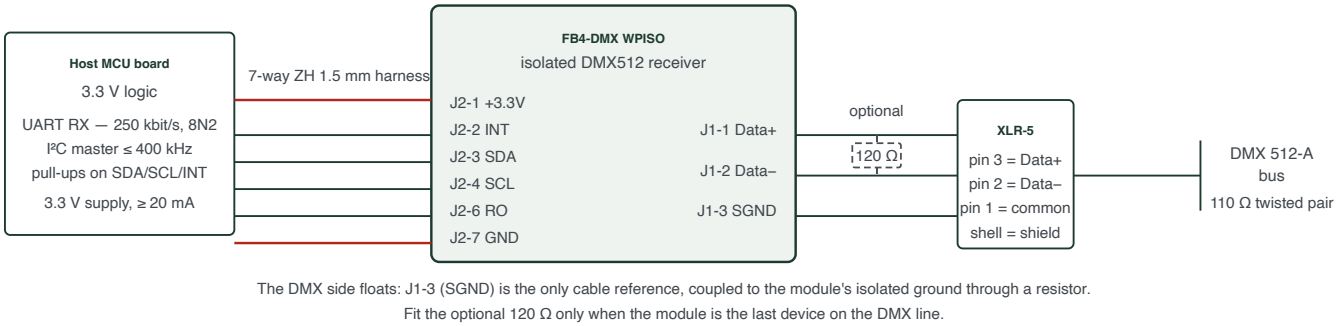

Figure 1 — Typical connection to a 3.3 V host and a DMX512-A line.

8.1 Application notes

- **Termination.** The module carries no 120 Ω terminator. If it is the last device on the line, fit 120 Ω across J1-1 and J1-2 in the harness or in the fixture. The on-board fail-safe bias does not replace termination.
- **Cable.** Use 110 Ω shielded twisted pair as required by ANSI E1.11. Land the shield on J1-3 at this end only; do not tie it to host ground.
- **Host pull-ups.** SDA, SCL and INT have no pull-up resistors on the module. Provide them on the host, typically 2.2 kΩ–4.7 kΩ to 3.3 V.
- **Supply.** Feed J2-1 from a clean 3.3 V rail. The isolated-supply converter draws a switched current; a local 10 µF ceramic on the host side of the harness is recommended if the harness is longer than ~150 mm.
- **Barrier keep-out.** On the host board and inside the enclosure, keep copper, wiring and metalwork away from the strip of PCB between the two domains.
- **Harness.** Both connectors are vertical-entry; the silkscreen note “双头同向” means the mating cable is built with both ends in the same orientation.

9 Mechanical data

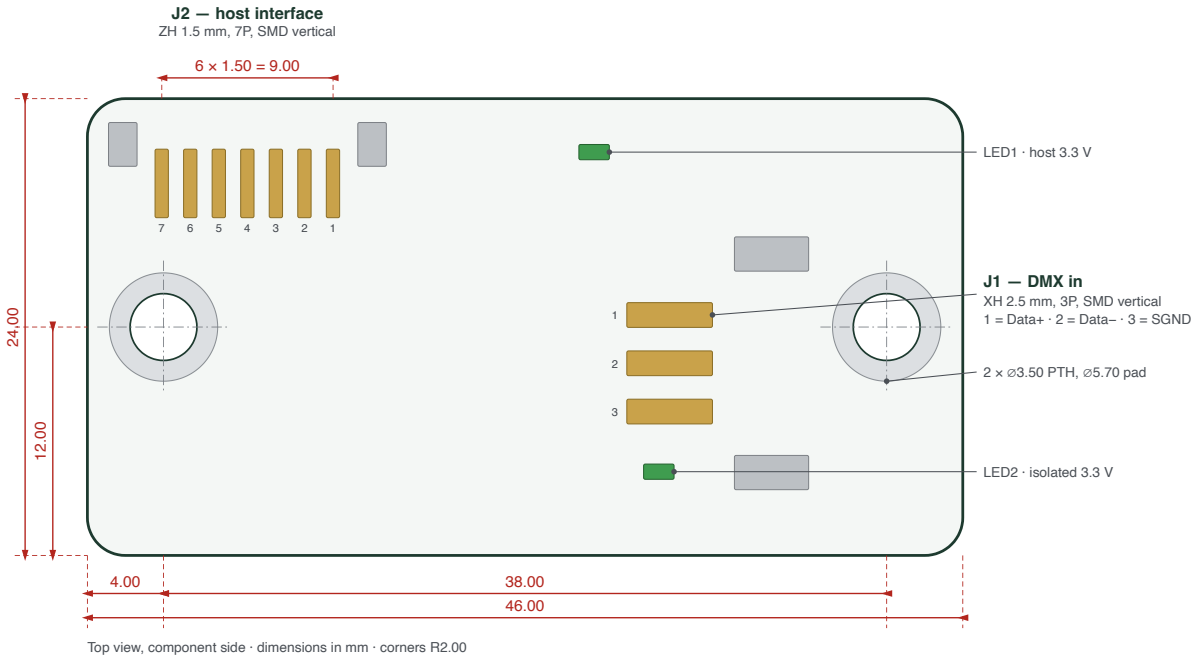

Figure 2 — Board outline and mounting, top view.

Parameter	Value
Board outline	46.00 × 24.00 mm, corners R2.00 mm
PCB	2-layer FR-4, 1.6 mm nominal, green solder resist, white legend
Mounting holes	2 × ø3.50 mm plated, ø5.70 mm annular pad, electrically floating
Hole positions	4.00 mm and 42.00 mm from the left edge, 12.00 mm from the bottom edge (38.00 mm centres, on the board centreline)
Tallest component	J1, 7.8 mm above the board surface
Component side	Single sided — all parts on the top layer
Edge finish	Depanelised from a stamp-hole panel; small break-off marks on the long edges are normal

10 Ordering and marking

Item	Value
Product name	FB4-DMX WPISO
Board revision	260820
Top-side marking	FB4 DMX WPISO / 20.Aug.2026
Delivery	Assembled and singulated boards; connectors fitted, harness not included

11 Revision history

Rev	Date	Change
A	2026-09-03	First issue. Describes board revision 260820.